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Ultralow Voltage Operation of p- and n-FETs Enabled by Self-Formed Gate Dielectric and Metal Contacts on 2D Tellurium

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The ongoing demand for more energy-efficient, high-performance electronics is driving the exploration of innovative materials and device architectures, where interfaces play a crucial role due to the continuous downscaling of device dimensions. Tellurium (Te), in its 2D form, offers significant potential due to its high carrier mobility and ambipolar characteristics, with the carrier type easily tunable via surface modulation. In this study, atomically controlled material transformations in 2D Te are leveraged to create intimate junctions, enabling near-ideal field-effect transistors (FETs) for both n-type and p-type operation. A $NiTe_x$-Te contact provides highly transparent interfaces, resulting in low contact resistance, while the TiO_x-Te gate dielectric forms an ultraclean interface with a capacitance equivalent to 0.88 nm equivalent oxide thickness (EOT), where the quantum capacitance of Te is observed. Subthreshold slopes (SS) approach the Boltzmann limit, with a record-low SS of 3.5 mV dec^{-1} achieved at 10 K. Furthermore, 2D Te-based complementary metal-oxide-semiconductor (CMOS) inverters are demonstrated operating at an ultralow voltage of 0.08 V with a voltage gain of 7.1 V/V. This work presents a promising approach to forming intimate dielectric/semiconductor and metal/semiconductor junctions for next-generation low-power electronic devices.

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Modern computational technology is experiencing a significant surge in power consumption driven by the increasing density and speed of electronic devices. As integrated circuits continue to evolve, the demand for higher performance pushes the limits of device scaling, leading to greater power dissipation and thermal challenges.[1] Among various approaches to enhance energy efficiency, scaling down the supply voltage V_{DD} has emerged as the most effective strategy, given that dynamic power consumption is proportional to the square of the supply voltage. This means even modest reductions in V_{DD} can lead to substantial power savings, making voltage scaling a key focus in the design of low-power electronics. However, reducing V_{DD} presents significant challenges, especially as complementary metal-oxide-semiconductor (CMOS) field-effect transistors (FETs) continue to downscale to atomic level. At these scales, the quality of interfaces between metal/semiconductor[2–11] and dielectric/semiconductor,[12–17] becomes critical in determining device performance.

In this paper, we present a simple and effective approach to achieving atomically sharp and ultraclean interfaces in 2D Te by precisely controlling chemical reactions and material transformations at the atomic scale. We demonstrate near-ideal n-type and p-type MOSFETs using 2D Te, featuring ultralow operation voltage CMOS inverters down to 0.08 V, negligible hysteresis, a gate capacitance equivalent to 0.88 nm equivalent oxide thickness (EOT), and a subthreshold slope approaching the Boltzmann limit in a wide temperature range. This study highlights the potential of 2D Te for next-generation low-power and cryogenic electronic applications, offering a pathway for reducing power consumption and enhancing device performance through advanced interface engineering.

1. 2D Te FETs with Self-Formed Metal Contacts and Gate Dielectrics

A 40 nm layer of Ti and Ni was directly deposited on top of 2D Te surface using electron-beam evaporation to form the top-gate

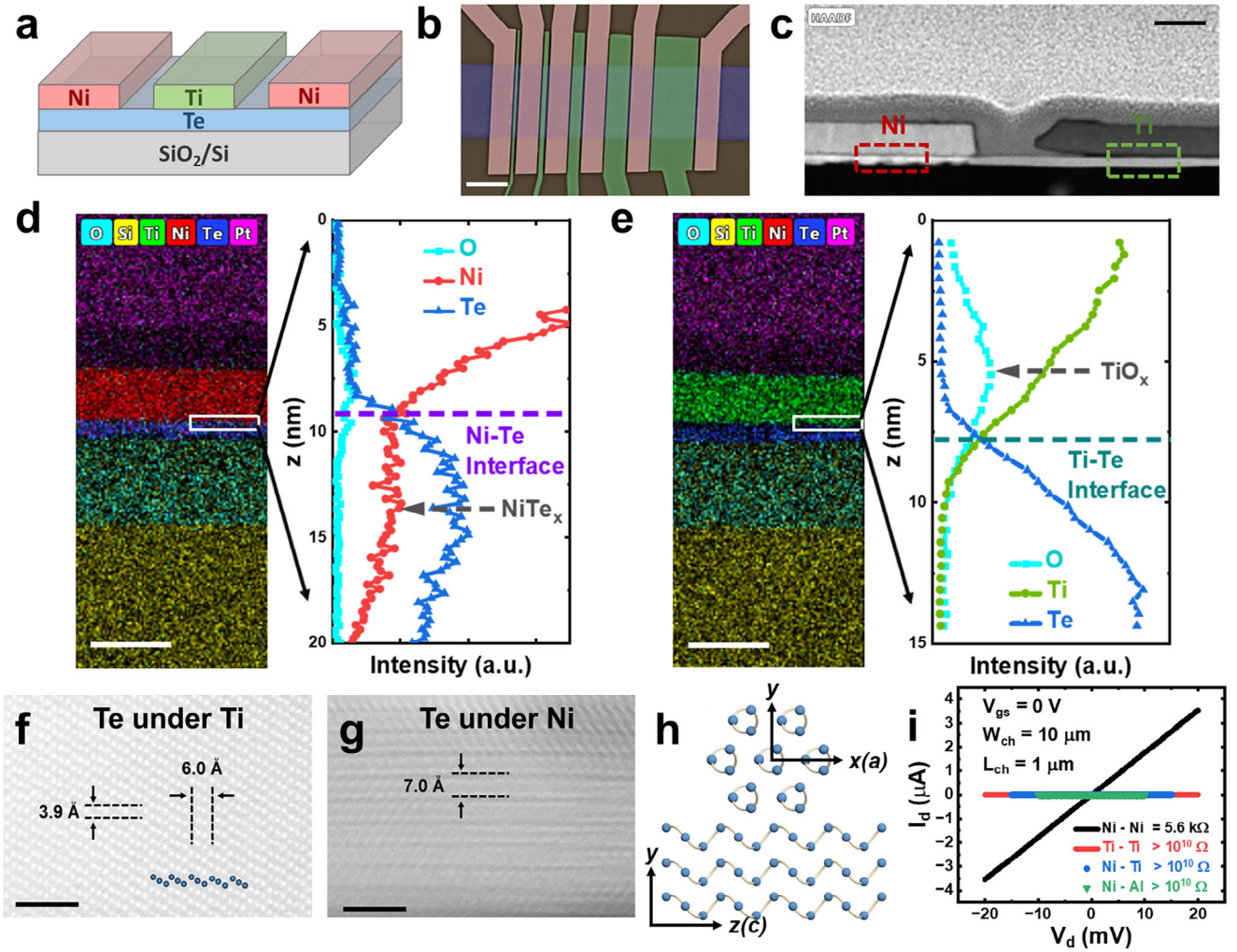

Figure 1. Atomically Sharp Self-Formed Metal Contacts and Gate Dielectrics in 2D Te. a) Schematic of a self-assembled 2D Te FET with directly deposited Ni as the contact and Ti as the gate. b) SEM image of a self-assembled 2D Te FET. The scale bar represents 2 μm. c) Cross-sectional HAADF-STEM image of the 2D Te FET. The scale bar represents 100 nm. d,e) EDS elemental mapping and line profiles at the Ni-Te (d) and Ti-Te (e) interfaces, indicating the formation of $NiTe_x$ metal contacts and TiO_x gate dielectrics. The scale bar represents 100 nm. f,g) STEM images showing crystallized $NiTe_x$ at the Ti gate region (f) and the Ni contact region (g). The scale bar represents 2 nm. h) Schematic of the crystal structure of 2D Te. i) Electrical properties of different metal-to-Te electrodes. Ti and Al exhibit insulating behavior, making them suitable for gate electrodes.

structure, as illustrated in **Figure** 1a. A 90 nm SiO_2/Si substrate was used as the back gate. 2D Te FETs with various gate lengths were fabricated, as shown in the scanning electron microscopy (SEM) image in **Figure** 2b. To characterize the material composition and device structure, high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) was performed. Figure 1c shows the cross-sectional HAADF-STEM image of a 2D Te FET device with Ni and Ti contacts, where a distinct contrast is observed beneath the Ni electrode, suggesting material chemical reaction and transformation occurred in 2D Te. To further investigate the difference between the Ni-Te and Ti-Te interfaces, energy dispersive x-ray spectroscopy (EDS) elemental mappings were conducted, as shown in Figure 1d,e. The line profiles across the interfaces reveal elemental distributions at the nanometer scale, clearly identifying the interfaces. The EDS mapping was possible by averaging over approximately 100 nm in length, thanks to the atomically sharp interface of the hydrothermally grown 2D Te. The Ni-Te interface shows a significant Ni signal within the Te region, indicating the formation of a Ni-Te compound. In contrast, the Ti signal decreases rapidly to zero within the Te region, suggesting minimal diffusion of Ti atoms. An oxygen peak is observed at the Ti interface, where the Te signal is absent, which is ascribed to the formation of a TiO_x layer. Te has a thin layer of self-formed and self-limited TeO_x native oxide at the surface,[18] which contributes to surface accumulation and results in the intrinsic p-type doping of 2D Te. The thickness of this TiO_x layer is estimated to be approximately 6 nm, based on the half-width of the peak. The formation of TiO_x can be attributed to the reduction of a thin layer of native TeO_x during the direct deposition of Ti. According to the Ellingham diagram,[19,20] which describes the Gibbs free energy (ΔG) of metal oxide formation, Ti is more reactive than Te at room temperature and has a stronger tendency to form oxides. No NiO_x layer is observed at Ni-Te interface. This thermodynamic preference results in the

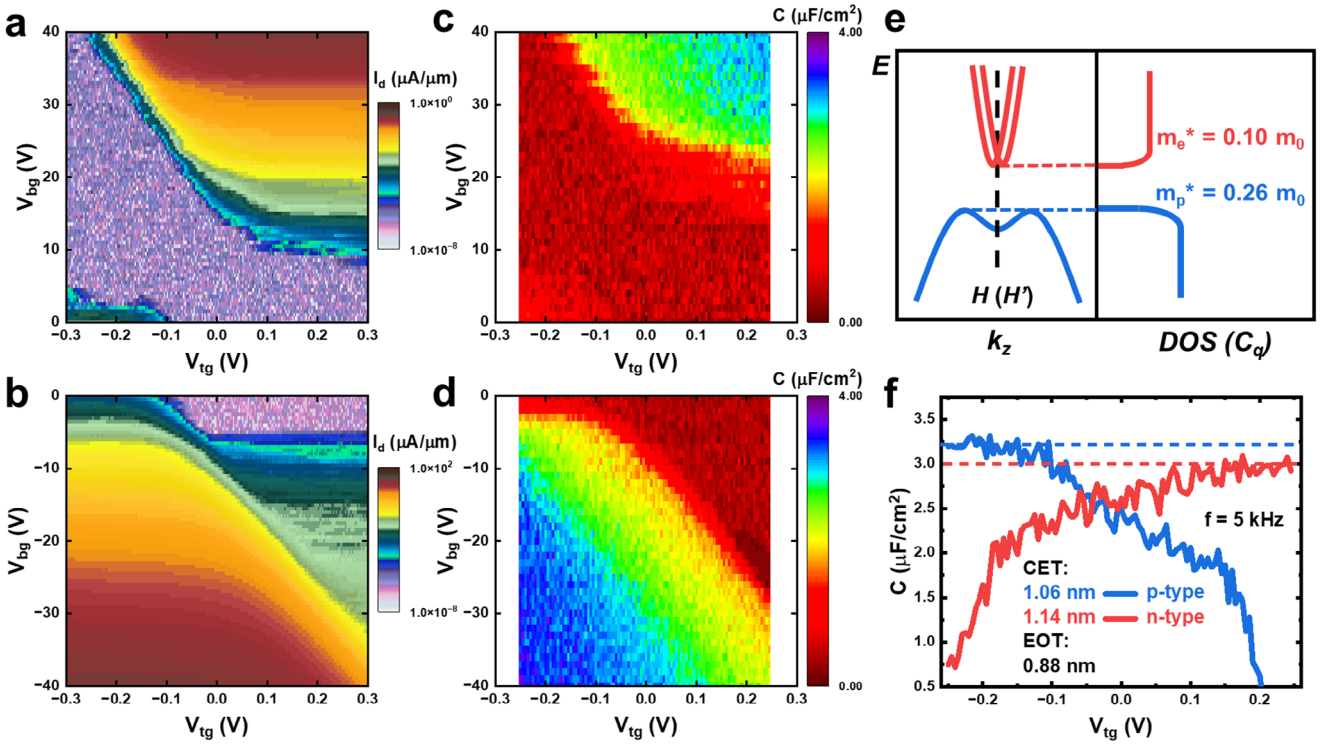

Figure 2. Highly Efficient Modulation of Carriers (Low CET) and Effects of Quantum Capacitance. a,b) Color maps of the drain current (I_d) as a function of back gate (90 nm SiO_2) voltage and top gate (self-assembled TiO_x) voltage, showing highly efficient modulation for both n-FET (a) and p-FET (b) in the same device. c,d) Color maps of the top gate capacitance (C) as a function of back gate and top gate bias. e) Schematic of Te band structure around the Fermi level. The differing effective masses at the conduction and valence bands result in distinct DOS and quantum capacitance (C_q). f) Capacitance versus top gate voltage for n-type and p-type Te in the same device, with CET values of 1.06 nm (p-type) and 1.14 nm (n-type). The difference in capacitance is attributed to the effect of quantum capacitance. The EOT of the top gate is extracted to be 0.88 nm.

formation of an insulating TiO_x layer that serves as a dielectric when Ti is deposited onto Te. Meanwhile, the process eliminates the native TeO_x which usually provides the significant interface traps.

Figure 1f,g shows HAADF-STEM images of 2D Te under Ti gate and Ni contact regions, respectively. Te possesses a unique chiral crystal structure, where three covalently bonded Te atoms in each unit cell form atomic chains along the c-direction. These atomic chains are arranged into a hexagonal lattice through van der Waals interactions. The single-crystalline Te structure with lattice constants of a = 4.5 Å and c = 6 Å, and a single atomic Te chain is highlighted in Figure 1f. The crystal orientation corresponds to the (1000) facet (y-z plane), as illustrated in Figure 1h. In contrast, 2D Te under the Ni contact undergoes a significant material transformation, displaying a completely different crystal structure from Te. A layered $NiTe_x$ structure with an interlayer spacing of 7 Å is observed, with the lattice constant of $NiTe_x$ varying depending on the material composition. The formation of $NiTe_x$ can be controlled by adjusting the annealing temperature and time after Ni deposition. Figure 1i shows the electrical properties of different metal electrodes on 2D Te. Similar to Ti, the Te-Al interface is also insulating due to the formation of Al_2O_3, making Ti and Al suitable for gate materials. The metallic nature of $NiTe_x$ makes it an excellent intimate contact[21] for semiconducting 2D Te, similar to contact doping in 2D materials[22,23] and silicides in Si-based technologies.[24] Figure S1 (Supporting Information) presents the HAADF-STEM image at the channel-to-contact region, revealing a sub-1 nm atomically sharp $NiTe_x$-Te interface. The contact length (L_c) corresponds to the thickness of the 2D Te layer. The specific contact resistivity (ρ_c) of p-type 2D Te FET is extracted to be $8.3 \times 10^{-8}\ \Omega\ cm^2$, which is very low among p-type FETs,[25,26] indicating that a clean and transparent semiconductor-to-metal interface is formed.

2. Device Performance of 2D Te FETs and Effects of Quantum Capacitance

Equivalent-oxide-thickness (EOT) is one of the important parameters of the dielectric layer in MOSFETs. Scaling EOT down to sub-one-nanometer region[13,27–30] with a low leakage current is critical to have a good electrostatic control of the semiconducting channel and a lower operating voltage. Here using the self-formed TiO_x as dielectric layer, we achieved an ultralow EOT of 0.88 nm and observed the quantum capacitance effect in 2D Te.

Figure 2a,b shows the color maps of drain current (I_d) as a function of top-gate (self-formed TiO_x) and back-gate (90 nm SiO_2) voltages for a 2D Te FET in n-type and p-type regions, respectively, at a temperature of 10 K. The 2D Te thickness is around 6 nm. Due to its narrow bandgap of 0.35 eV,[31] the carrier type in 2D Te can be effectively tuned via electrical gating. The transfer curves are presented in Figure S2a (Supporting Information). Comparing the drain current responses, the top-gate

is ≈100 times more efficient than the back-gate in transconductance; specifically, a gate voltage change of 0.1 V at the top-gate yields the same current level as 10 V change at the back-gate. Notably, there is a difference in efficiency between the p-type and n-type regions. It is important to note that the top-gate and back-gate are not identical in terms of interface conditions. The back-gate interacts through van der Waals forces, while the top-gate involves a deposition process. Additionally, the contact region is influenced by the back gate, with a connecting region between the contact and the top-gate. Another representative device exhibiting similar behavior and top-gate tunability is shown in Figure S2 (Supporting Information).

Using the same device structure, the capacitance of top gate was measured as a function of top-gate and back-gate voltages, with the Ni electrode grounded, for both n-type and p-type 2D Te FET, as shown in Figure 2c,d, respectively. The capacitance maps exhibit similar behavior to the drain current maps, displaying distinct depletion and accumulation regions. The capacitance-equivalent-thickness (CET) reflects the tunability of the dielectrics integrated with the semiconductor. Typically, CET is higher than EOT due to the quantum capacitance (C_q) effect.[32] In conventional Si-based MOSFETs, the quantum capacitance is relatively large, making the total gate capacitance close to the oxide capacitance (C_{ox}). However, quantum capacitance effects become significant when materials exhibit unique DOS versus energy dispersion, as seen in graphene and carbon nanotubes,[33,34] and when the oxide capacitance is sufficiently large. In 2D Te, the narrow bandgap enables access to the transport properties of both the conduction and valence bands within the same device. Since the gate stack and total capacitance remain unchanged, while the quantum capacitance differs, the effects of quantum capacitance become distinguishable. This distinction is further enhanced by the high mobility or low effective mass of carriers on both sides. Figure 2e illustrates the band structure of 2D Te near the Fermi level. The conduction band minimum and valence band maximum are located around the H (H') point with twofold valley degeneracy. Due to the three-fold screw symmetry and the strong spin-orbit coupling, the spin degeneracy of the conduction band splits and crosses at the H (H') point, forming a Weyl node.[35] The valence band also exhibits spin non-degeneracy with a camel-back structure. The quantum capacitance is directly proportional to the DOS and, under a parabolic approximation, can be expressed as:

$$C_q = \rho\, e^2 = \frac{g_s g_v m^* e^2}{2\pi\hbar^2} \tag{1}$$

where ρ is the density of states, g_s and g_v is the spin and valley degeneracies, respectively, and m^* is the effective mass. For valence band, $g_{sp} = 1$, $g_{vp} = 2$, and $m_p^* = 0.26m_0$,[36] resulting in $C_{qp} = 17.52\ \mu F/cm^2$. For conduction band, $g_{sn} = 2$, $g_{vn} = 2$, and $m_n^* = 0.10m_0$,[35,37] resulting in $C_{qn} = 13.48\ \mu F/cm^2$. It is noteworthy that at lower carrier densities, due to the spin-orbit coupling, the band deviates from a parabolic shape near the band edge,[38] making the parabolic approximation valid only at high carrier densities. We observed an increase in capacitance with applied voltage when the device had relatively low carrier densities and used the final saturated capacitance to calculate the quantum capacitance. The CET for p-type and n-type regions at high densities is extracted to be 1.06 and 1.14 nm, respectively in the same device, as shown in Figure 2f. Considering the quantum capacitance effect, the EOT of the same gate is calculated to be 0.88 nm for both p-type and n-type regions, providing strong evidence for the presence of quantum capacitance effects. The observed increase in capacitance at higher carrier densities further supports the spin-orbit interaction-induced quantum capacitance effect.

The self-formed Ti gate can also function as a back-gate where the TiO_x is formed during the sample fabrication, mitigating limitations associated with the resistance of the contact and the contact-to-gate connecting region. The threshold voltage (V_t) is controlled by growing a thin layer of Al_2O_3 (1 to 3 nm) on the Te surface,[39] effectively removing the intrinsic doping effects from the native tellurium oxide layer. Utilizing highly transparent metal contacts and efficient gate dielectrics, the electrical performance of the self-formed 2D Te n-FET and p-FET devices, each with a channel length of 1 μm at 33 K, is presented in **Figure 3**a,b and Figure 3c,d, respectively. Both n- and p-type devices exhibit an on/off current ratio of 10^6 at $V_{ds} = 0.05$ V, demonstrating excellent switching behavior. An on-current of 11 μA μm^{-1} is achieved with well-defined saturation behavior at $V_{ds} = 0.5$ V and $V_{gs} = 0.5$ V, demonstrating the potential for low-voltage V_{DD} of 0.5 V operation. Moreover, the devices exhibit ultralow hysteresis of 4 and 2 mV at the 10^{-5} μA μm^{-1} current level in n-FET and p-FET configurations, respectively. This low hysteresis reflects the presence of a clean dielectric-to-semiconductor interface, resulting a low density of interfacial traps and enhanced device stability. The room temperature device behavior is shown in Figure S3 (Supporting Information), the on/off ratio is limited by the narrow bandgap. Further reducing the thickness and introducing Se doping can improve the on/off ratio. The Al gate has a better leakage current than the Ti gate due to the bandgap difference, further engineering can be done by co-evaporating Al and Ti to improve the leakage current.

3. Ultralow Voltage Operation of 2D Te CMOS Inverters Enabled by the Ultraclean Interfaces

The ultraclean dielectric-to-semiconductor interface enables improved control of switching in the subthreshold region. **Figure 4**a presents the transfer curves of a 1 μm channel length device at $V_{ds} = 0.01$ and 0.05 V at 10 K. The transistors exhibit a steeper slope in the subthreshold region, with the device undergoing a 6-order-of-magnitude change in resistance within a 0.2 V gate voltage window. The subthreshold slope (SS) is calculated using the relation $SS = \partial log(I_d)/\partial V_{gs}$ at different current levels, as shown in Figure 4b. An ultralow SS of 3.5 mV dec^{-1} is achieved. Figure 4c,d displays the temperature dependence of the transfer characteristics for the 2D Te n-FET and p-FET, respectively, from 10 to 295 K. The extracted SS values are summarized in Figure 4e. The subthreshold slope can be expressed as: $SS = \ln(10)\frac{nkT}{q}$, $n = 1 + \frac{C_d + C_{it}}{C_{ox}}$, where k is the Boltzmann constant, q is the elementary charge, T is temperature, C_d is depletion layer capacitance, C_{it} is interfacial trap capacitance, C_{ox} is oxide capacitance.[14] In 2D Te, the SS is close to the Boltzmann limit ($n = 1$) and scales linearly with temperature in both n-type and p-type transistors under 200 K, indicating low interfacial trap states and high gate oxide capacitance. At higher temperatures (above

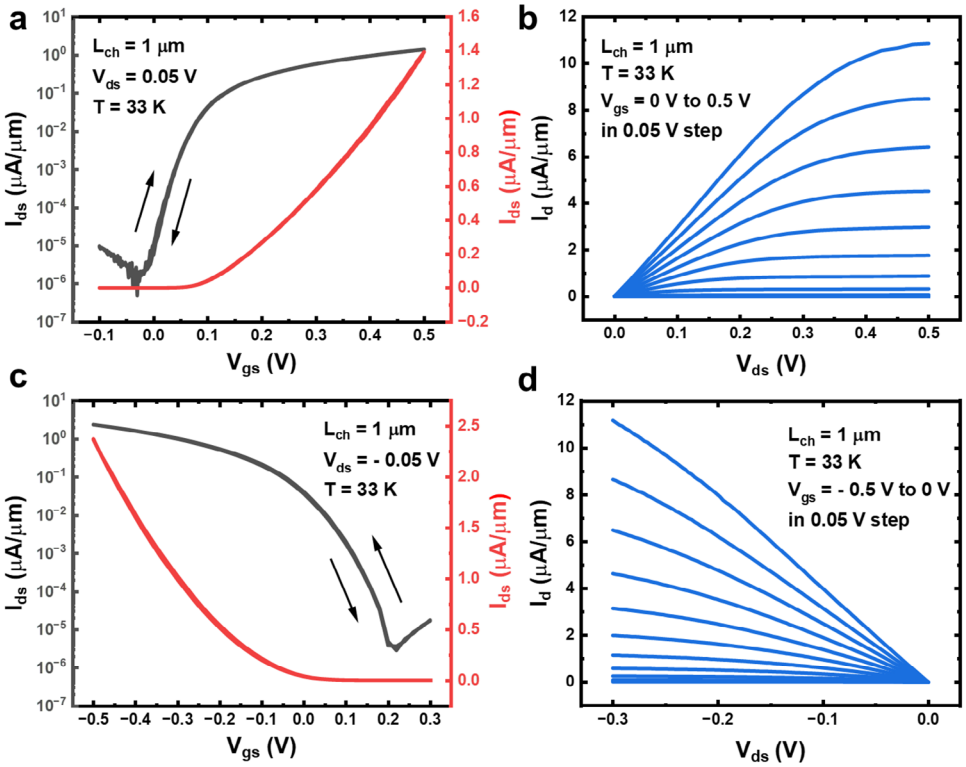

Figure 3. Low Voltage Operation of 2D Te n- and p-FETs Using Ti as Back Gate. a) Transfer characteristic of a 2D Te n-FET with a 1 μm channel length at 33 K. The n-type doping is achieved by depositing 3 nm Al_2O_3 via ALD on the 2D Te surface. b) Output characteristic of the same n-FET device shown in (a), demonstrating good saturation behavior. c) Transfer characteristic of a 2D Te p-FET with a 1 μm channel length at 33 K. d) Output characteristic of the same p-FET device shown in (c).

200 K), the SS deviates from the Boltzmann limit due to the thermal activation of electrons and holes in p- and n-FETs, owning to the narrow bandgap of Te. Notably, the SS in 2D Te does not saturate as temperature decreases, unlike Si-based FETs, which exhibit saturation at cryogenic temperatures (4.5 mV dec^{-1} at 4 K).[40] In Si, band-tail states limit the further reduction of SS at low temperatures; however, Te offers the potential for continued SS scaling under such conditions. This makes 2D Te MOSFETs a promising candidate for cryogenic-temperature computing.

2D Te FETs can be modeled as two back-to-back Schottky diodes in the thermionic emission regime. The barrier height Φ_B is extracted from temperature-dependent measurements using: $I_d \approx A^* T^{1.5} \exp\left(-\frac{q\Phi_B}{kT}\right)$, with $q\Phi_B = q\Phi_{B0} - \frac{V_{gs}-V_{FB}}{n}$ for $V_{gs} < V_{FB}$, where A^* is the Richardson constant, V_{FB} is flat band voltage.[7] The gate-dependent barrier height, shown in Figure 4f, is calculated from the slope of the Arrhenius plots (Figure S4, Supporting Information). The n factor is extracted to be 1.05 for n-FET and 0.93 p-FET based on barrier heights at $V_{gs} < V_{FB}$, providing further evidence of the ultraclean semiconductor-to-dielectric interface. The Schottky barrier height is extracted to be 38.7 and 21.7 mV for n-type and p-type transistors, respectively, at the flat band condition. In contrast to most of the 2D materials[41] or Ge-based devices,[42] where contacts suffer from large Schottky barriers due to the Fermi level pinning effect at the semiconductor-to-metal interface, the $NiTe_x$-Te interface offers near transparent contacts for both electrons and holes.

The near-ideal n-FETs and p-FETs based on 2D Te pave an alternative path for scaling down V_{DD} of CMOS technology, thereby reducing power consumption. **Figure** 5a shows the voltage transfer characteristics of a 2D Te CMOS inverter at 10 K for different V_{DD} values. A common input and output electrode structure is employed with the threshold voltage controlled by ALD capping of Al_2O_3. The device demonstrates ultralow operating voltage with V_{DD} = 0.08 V, exhibiting full-output-swing behavior. The inverter gain ($\partial V_{out}/\partial V_{in}$) is presented in Figure 5b, where a high gain of 7.1 V/V is achieved at V_{DD} = 0.08 V. Butterfly curves (Figure S5, Supporting Information) with two storage states represent the performance of two cross-coupled inverters, which serve as the fundamental building blocks for static-random-access memory (SRAM). The noise margin dependence on V_{DD} is extracted using the largest possible square method and is plotted in Figure 5b. A significant noise margin of 75% is achieved, highlighting the potential for stable and reliable low-voltage operation in 2D Te-based CMOS technology.

4. Conclusion

The formation of intimate interfaces through self-formed materials via direct metal deposition on 2D Te provides a novel approach to achieving near-ideal n-type and p-type MOSFETs. This strategy enables ultralow operating voltages of 0.08 V and a voltage gain of 7.1 V/V in 2D Te CMOS inverters, facilitated by the transparent metal/semiconductor $NiTe_x$-Te contacts and

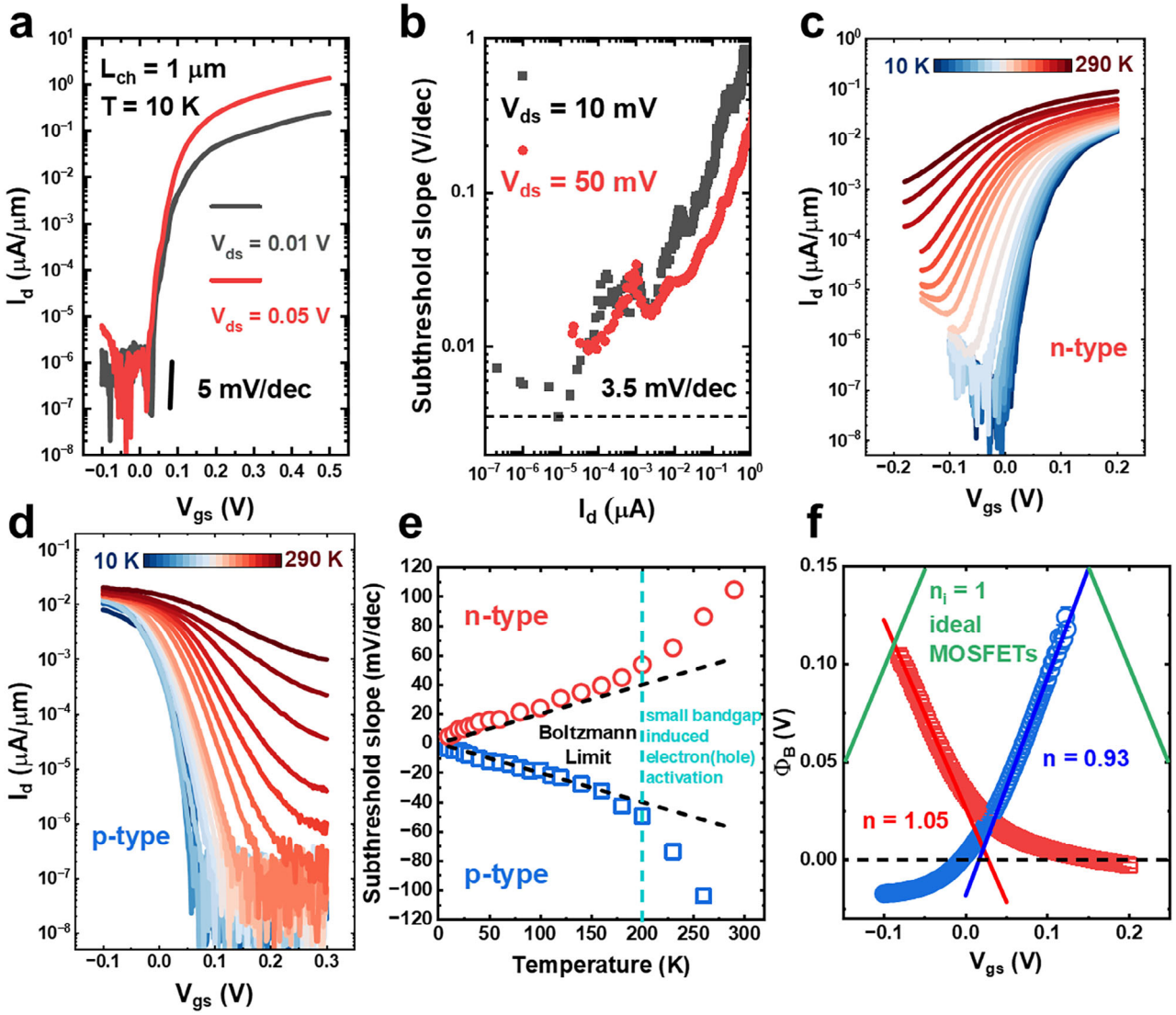

Figure 4. Near-Ideal Subthreshold Slope (SS) in 2D Te n- and p-FETs Enabled by Ultraclean Self-Formed Semiconductor-to-Dielectric Interface. a) Transfer characteristic of a 2D Te n-FET at 10 K under different V_{ds}. b) Subthreshold slope (SS) as a function of the drain current, demonstrating an ultralow SS of 3.5 mV dec^{-1}, indicative of the ultraclean interface. c,d) Temperature dependence of transfer characterizations for n-FET (c) and p-FET (d). e) SS of 2D Te n- and p-FET as a function of temperature. The SS closely follows the Boltzmann limit below 200 K, with deviations at higher temperatures attributed to the thermal activation of electrons in p-FETs and holes in n-FETs. f) Barrier height as a function of gate voltage extracted from (c) and (d), demonstrating near-ideal gate tunability in both p-FET and n-FET.

ultraclean dielectric/semiconductor TiO_x-Te interfaces. The TiO_x-Te interfaces exhibit low interfacial trap states and an ultrahigh gate capacitance with an equivalent oxide thickness (EOT) of 0.88 nm. Our findings present a scalable pathway for significantly reducing power consumption in future CMOS technologies by precisely engineering metal-semiconductor and dielectric-semiconductor interfaces.

5. Experimental Section

Hydrothermal Growth of 2D Te flakes: One gram of polyvinylpyrrolidone (PVP) (Sigma–Aldrich) and 0.18 g of Na_2TeO_3 (Sigma–Aldrich) were dissolved in 64 mL double-distilled water. 6.66 mL of aqueous ammonia solution (25–28%, w/w%) and 3.34 mL of hydrazine hydrate (80%, w/w%) were added to the solution under magnetic stirring to form a homogeneous solution. The mixture was sealed in a 100 mL Teflon-lined stainless-steel autoclave and heated at 180 °C for 20 h before naturally cooling down to room temperature.

Device Fabrication: Te flakes were transferred onto 90 nm SiO_2/Si substrate or prepatterned 40 nm Ti substrate using Langmuir-Blodgett method. The 2D Te FETs were patterned using electron beam lithography and metal contacts (Ni) and gate dielectric (Ti and Al) were deposited by electron beam evaporation. Optional 3 nm atomic layer deposition (ALD) grown Al_2O_3 was used to tune the threshold voltage of the 2D Te FETs at 120 °C using $(CH_3)_3Al$ (TMA) and H_2O as precursors.

High Resolution Scanning Transmission Electron Microscopy (HR-STEM): TEM, selected area diffraction, energy dispersive x-ray spectroscopy (EDS) elemental mappings, and HAADF-STEM analysis were performed with FEI TALOS F200x. This microscope was operated with an acceleration voltage of 200 kV.

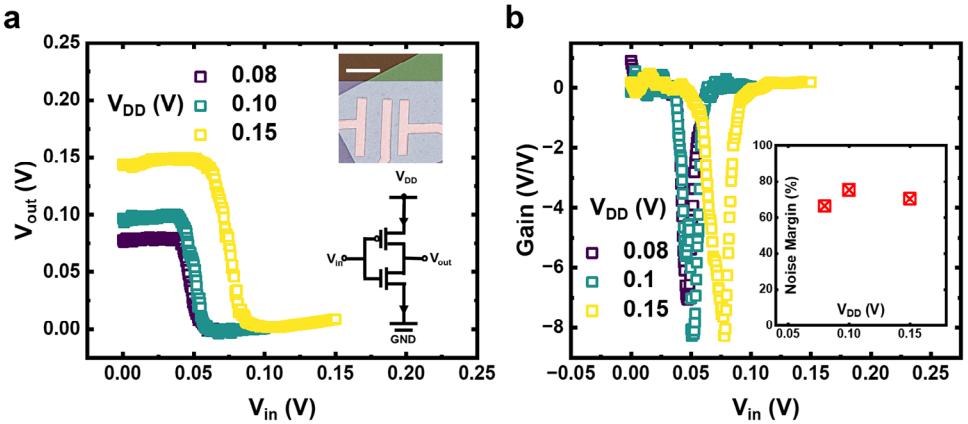

Figure 5. Ultralow Voltage Operation of 2D Te CMOS Inverters. a) Voltage transfer characteristic of a typical 2D Te CMOS inverter operating at an ultralow voltage of 0.08 V. Inset: SEM image and schematic of the 2D Te CMOS inverter. The scale bar represents 5 µm. b) Voltage gains at different V_{DD} extracted from (a). A high gain of 7.1 V/V is achieved at 0.08 V V_{DD}. Inset: Noise margin of the inverter at different V_{DD}. The measurement temperature is 10 K.

Low-Temperature Electrical Measurements: The low temperature characterization was performed in a Lakeshore CRX-VF cryogenic probe station. The electrical characterization of transistors and inverters was measured with the Keysight B1500 system. The capacitance versus voltage measurements were performed using Agilent E4980A LCR Meter at an excitation of 20 mV.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

C.N. and L.L. contributed equally to this work. P.D.Y. supervised the project. C.N. and L.L. designed the experiments. L.L., C.N., Z.L., and J.-Y.L. fabricated the devices. L.L., C.N., P.T., and W.W. synthesized the materials. Y.Z. and H.W. carried out the TEM/STEM measurements and image analysis. C.N. and L.L. performed the electrical measurements and analyzed the data. P.D.Y., C.N., and L.L. wrote the manuscript and all the authors commented on it.

Data Availability Statement

Research data are not shared.

Keywords

2D Tellurium, contact, dielectric, n-FET, p-FET

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